AF/2814

PTO/SB/21 (04-04)
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(to be used for all correspondence after initial filing)

Application Number	09/804,004
Filing Date	12 March 2001
First Named Inventor	Marcel Eduard Irene Broekaart
Art Unit	2814
Examiner Name	Nathan Ha
Total Number of Pages in This Submission: 18	Attorney Docket Number: NL000314

ENCLOSURES *(Check all that apply)*

- [X] Fee Transmittal Form
  - [X] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
- [ ] After Allowance communication to Technology Center (TC)
- [ ] Appeal Communication to Board of Appeals and Interferences
- [X] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [X] Other Enclosure(s) (please Identify below): 2 return post cards

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Raymond J. Werner
Signature	Raymond J. Werner Reg. No. 34,752
Date	29 Sept. 2004

CERTIFICATE OF TRANSMISSION/MAILING

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Typed or printed name	Raymond J. Werner		
Signature	Raymond J. Werner	Date	29 Sept 2004

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PTO/SB/17 (10-03)
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FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 330 —

Complete If Known	
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Filing Date	12 March 2001
First Named Inventor	Marcel Eduard Irene Broekaart
Examiner Name	Nathan Hla
Art Unit	2814
Attorney Docket No.	NL000314

METHOD OF PAYMENT *(check all that apply)*

☒ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☐ Deposit Account:

Deposit Account Number

Deposit Account Name

The Director is authorized to: *(check all that apply)*

☐ Charge fee(s) indicated below ☐ Credit any overpayments

☐ Charge any additional fee(s) or any underpayment of fee(s)

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 0

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

	Extra Claims		Fee from below		Fee Paid
Total Claims		-20** =		X	=
Independent Claims		- 3** =		X	=
Multiple Dependent					=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	330
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid SUBTOTAL (3) ($) 330 —

SUBMITTED BY

(Complete *(if applicable)*)

Name (Print/Type)	Raymond J. Werner	Registration No. (Attorney/Agent)	34752	Telephone	503-466-2994
Signature	Raymond J. Werner			Date	29 Sept. 2004

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant	:	Marcel Eduard Irene Broekaart ;	
Appl. No.	:	09/804,004 ;	Grp./Art Unit : 2814
Filed	:	12 March 2001 ;	Examiner: Nathan Ha
Title	:	Method Of Manufacturing A Semiconductor Device ;	
Docket No.	:	NL 000314 ;	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Sir:

This Appeal Brief is being filed in response to the Examiner's Final Rejection of Claims 1 and 3-16. A Notice of Appeal was filed on 04 August 2004.

Real Party In Interest

The real parties in interest in this application are the assignee, U. S. Philips Corporation, and Koninklijke Philips Electronics N.V., which is the parent company of the assignee.

Related Appeals or Interferences

Applicant is not aware of any related appeals or interferences.

Status of Claims

Claims 1 and 3-16 are pending in the application, Claim 2 was previously cancelled, and all the pending Claims 1 and 3-16 have been finally rejected. The rejection of Claims 1 and 3-16 is being appealed.

Status of Amendments

All previously filed amendments are believed to have been entered. Responsive to Applicants' After Final Response of 18 June 2004, an Advisory Action dated 08 July 2004, in numbered paragraph (7), indicates that, for purposes of Appeal, the proposed amendments will be entered. However, Applicants' After Final Response of 18 June 2004 contained no amendments.

Summary of Claimed Subject Matter

A concise explanation of independent Claims 1 and 13, as required under 37 CFR §41.37(c)(1)(v), is provided below.

Briefly, independent Claim 1 defines a semiconductor manufacturing process, in which a patterned conductor is disposed on a semiconductor substrate, an etch stop layer is formed on the top and sidewall surfaces of the patterned conductor, a dielectric layer is applied over the etch stop layer, a via is etched through the dielectric layer overlying the conductor with this etch process stopping on the etch stop layer, the exposed etch stop layer is removed, and the via is filled with a

conductive material. Figs. 1-4 are cross-sectional views illustrating intermediate structures formed during the claimed process. Each of Figs. 1-4 show that etch stop layer 12 is formed such that no other layer is disposed between etch stop layer 12 and any of the conductive layers 3, 4, or 5. This process is generally described in the specification at page 3, line 6 through page 6, line 17; and more particularly, the formation, location, and composition of etch stop layer 12 in particular can be found at page 4, lines 5-9.

Briefly, independent Claim 13 defines a semiconductor manufacturing process for forming electrically conductive pathways, for example, vias between metal interconnect levels in an integrated circuit. The claimed process includes forming a patterned conductor that has a capping layer thereon; forming a conformal etch stop layer over the top and side surfaces of patterned conductor and capping layer; forming a dielectric layer over the etch stop layer; exposing a portion of the etch stop layer by forming a via opening, the via opening at least partially overlapping the patterned conductor; anisotropically etching the exposed portion of the etch stop layer such that at least a portion of the capping layer is exposed; and filling the via opening with electrically conductive material. Figs. 1-4 are cross-sectional views illustrating intermediate structures formed during the claimed process. Each of Figs. 1-4 show that etch stop layer 12 is formed such that no other layer is disposed between etch stop layer 12 and any of the conductive layers 3, 4, or 5, and Figs. 3 and 4 show that, with respect to conductor 4, a portion of the capping layer (at top surface 6) is exposed. This process is generally described in the specification at page 3, line 6 through page 6, line 17; and more particularly, the removal of portions of etch stop layer 12 can be found at page 5, line 25 through page 6, line 5.

Grounds of Rejection To Be Reviewed On Appeal

1) Claims 1, 3-5, 9, and 12 have been rejected under 35 USC §102(e) as being anticipated by Avanzino, et al. (US Patent 6,593,632).

2) Claims 13-14 have been rejected under 35 USC §102(e) as being anticipated

by Wolstenholme (US Patent 6,649,968).

3) Claims 7-8 and 10 have been rejected under 35 USC §103(a), as being unpatentable over Avanzino, et al., as applied to Claims 1, 3-5,9 and 12, in view of Boeck, et al., (US Patent 5,880,018).

4) Claims 6 and 11 have been rejected under 35 USC §103(a), as being unpatentable over Avanzino, et al., in view of Ngo, et al., (US Patent 6,190,966).

5) Claim 15 has been rejected under 35 USC §103(a), as being unpatentable over Wolstenholme as applied to Claims 13-14, and further in view of Avanzino, et al.

6) Claim 16 has been rejected under 35 USC §103(a), as being unpatentable over Wolstenholme and Avanzino, et al., as applied to Claims 15, and further in view of Boeck, et al.

Argument

Rejection of Claims 1, 3-5, 9, and 12

Claims 1, 3-5, 9, and 12 have been rejected under 35 USC §102(e) as being anticipated by Avanzino, et al., (US Patent 6,593,632).

For the reasons set forth below, Applicants respectfully submit that the recited limitations of independent Claim 1 are not disclosed, suggested, or motivated by Avanzino, et al. Similarly, Applicants submit that the limitations of Claims 3-5, 9, and 12, which depend, directly or indirectly, from Claim 1, are neither disclosed, suggested, or motivated by Avanzino, et al.

Avanzino, et al., disclose forming a silicon carbide etch stop layer 21 over the top surface of gate electrodes 16, 17, and over the sidewall spacer structures 20 that are formed adjacent to the gate electrodes 16, 17.

Avanzino, et al., do not disclose, suggest, or provide motivation for the invention defined by Applicants' Claim 1. The disclosure of Avanzino, et al., does not disclose applying the etch stop layer to the conductor sidewalls. Rather,

Avanzino, et al., disclose that the etch stop layer is separated from the conductor sidewalls by a sidewall spacer (Fig. 1, element 20; and column 4, lines 10-12).

The invention defined by Applicants' Claim 1 requires that the etch stop layer be applied to the sidewall portions of the conductor. The sidewall portions of the conductor (reference numeral 7 in Applicants' Figs. 1, 3 and 4) are clearly shown by Applicant to be the side surfaces of the conductors.

Applicants respectfully assert that a "sidewall spacer" is a very well-known structure in the field of semiconductor manufacturing. Avanzino, et al., disclose forming an etch stop layer on sidewall spacers and not on the sidewalls of a conductor. The Examiner appears not to distinguish between the sidewall (i.e., the side surfaces) of a structure, and a sidewall spacer that may be formed adjacent to the sidewall of a structure.

In view of the foregoing Applicants respectfully submit that the rejection of Claim 1 under 35 USC 102(e) is improper and should be reversed. Similarly, Applicants submit that the rejections of Claims 3-5, 9 and 12, which depend directly or indirectly from previously presented Claim 1, are also improper and should be reversed.

Rejection of Claims 13 and 14

Claims 13-14 have been rejected under 35 USC §102(e) as being anticipated by Wolstenholme (US Patent 6,649,968).

For the reasons set forth below, Applicants respectfully submit that the recited limitations of independent Claim 13, and of Claim 14 which depends from Claim 13, are not disclosed, suggested, or motivated by Wolstenholme.

Applicants' independent Claim 13 recites that an electrically conductive capping layer is disposed on the top surface of the patterned conductor. The structure of Wolstenholme referred to by the Examiner (i.e., element 23 of Fig. 9) is actually a floating gate. A floating gate by definition is electrically isolated, and therefore does not have an electrically conductive capping layer disposed on the top

surface thereof. It is well-known in the semiconductor manufacturing arts that a floating gate is not in contact with any other electrically conductive element. Applicants' claimed process simply cannot produce the structure disclosed by Wolstenholme.

The Examiner has mischaracterized element 42 in Fig. 9 of Wolstenholme, as being the same as the sidewall of a patterned conductor in Applicants' Claim 13. This is incorrect because element 42 of Fig. 9 is actually a sidewall spacer and not the sidewall (i.e., side surface) of a conductor as recited by Applicants' Claims.

The Examiner has mischaracterized the photoresist layer 48 in Figs. 8 and 9 as the dielectric layer of Applicants' Claims. To say the least, this is an uncommon interpretation of the terms.

The Examiner has mischaracterized element 46 of Figs. 8 and 9, as an etch stop layer, when in fact it is an "insulative sidewall forming layer" (see Wolstenholme, col. 7, lines 61-63). In other words, this is the layer from which sidewall spacers are formed. As noted above, Applicants' claimed invention requires the etch stop layer to be formed on the conductor sidewalls, not on sidewall spacers.

In view of the foregoing it can be seen that the recitations of independent Claim 13, e.g., a conductor with a capping layer, an etch stop layer in contact with the sidewalls of the conductor and capping layer, and a dielectric layer over the etch stop layer are not found in Wolstenholme.

Applicants respectfully submit that the rejection of Claims 13-14 under 35 USC §102(e) is improper and should be reversed.

Rejection of Claims 7-8 and 10

Claims 7-8 and 10 have been rejected under 35 USC §103(a), as being unpatentable over Avanzino, et al., as applied to Claims 1, 3-5,9 and 12, in view of Boeck, et al., (US Patent 5,880,018).

For the reasons set forth below, Applicants respectfully submit that the recited limitations of Claims 7-8 and 10, which depend directly or indirectly from

independent Claim 1, are not disclosed, suggested, or motivated by the combination of Avanzino, et al., and Boeck, et al.

The Examiner has rejected these Claims stating the Avanzino, et al., discloses the claimed invention except for a capping layer, and Boeck, et al., is cited for element 64 in Fig. 15 thereof, to show a capping layer.

As discussed above, independent Claim 1 has been improperly rejected in view of Avanzino, et al., because the recited features of Claim 1 (e.g., applying the etch stop layer to the conductor sidewalls) are not disclosed by Avanzino, et al. Rather, Avanzino, et al., disclose that the etch stop layer is separated from the conductor sidewalls by a sidewall spacer (Fig. 1, element 20; and column 4, lines 10-12). Since Claims 7-8 depend, directly or indirectly, from Claim 1, the rejection of these Claims based on Avanzino, et al., is defective.

Furthermore, the Examiner has incorrectly characterized the barrier layer 64 of Boeck, et al., as the capping layer recited in Applicants' Claims. It is clear that the barrier layer 64 of Boeck, et al., is different from the capping layer illustrated and described in Applicants' patent application (see, for example, elements 8, 9, and 10, in Figs. 1-4). The barrier layer 64 of Boeck, et al., covers only a portion of the conductor top surface, which is inherently not the function of a capping layer. Applicants' use of the expression "capping layer" is well-understood in the semiconductor manufacturing arts to represent a layer that covers a complete surface of a structure, and not only a partial surface of that structure.

Furthermore, the barrier layer 64 of Boeck, et al., does not have its surface covered by the etch stop layer, as is clearly called for by the recitations of Claim 7. In other words, Claim 7 says that the top surface of the conductor is the top surface of the capping layer, while Claim 1 recites that the etch stop layer is on the top surface of the conductor. Clearly, Boeck, et al., do not disclose the features of Applicants' Claims.

In view of the foregoing, Applicants respectfully submit that the rejection of Claims 7-8 is improper and should be reversed.

Rejection of Claims 6 and 11

Claims 6 and 11 have been rejected under 35 USC §103(a), as being unpatentable over Avanzino, et al., in view of Ngo, et al., (US Patent 6,190,966).

Both Claims 6 and 11 depend directly from Claim 1, which Applicants have shown above is not disclosed, suggested, or motivated by Avanzino, et al. Claims 6 and 11 recite various metals which may be used to form the conductor and the via. The Examiner cites Ngo, et al., for the disclosure of tungsten in a via opening. Applicants respectfully assert that the combination Avanzino, et al., and Ngo, et al., do not disclose, suggest, or provide motivation for the claimed invention, and therefore this improper rejection should be reversed. In fact, Ngo, et al., show a sidewall spacer separating an etch stop layer from the sidewall of a conductor, which, as noted, is unlike Applicants' claimed invention in which the etch stop layer is formed adjacent the conductor sidewalls without any intervening sidewall spacer.

In view of the foregoing, Applicants respectfully submit that the rejection of Claims 6 and 11 is improper and should be reversed.

Rejection of Claim 15

Claim 15 has been rejected under 35 USC §103(a), as being unpatentable over Wolstenholme, as applied to Claims 13-14, and further in view of Avanzino, et al.

Claim 15 depends indirectly from Claim 13, which Applicants have argued above is not disclosed, suggested, or motivated by Wolstenholme. The Examiner cites Avanzino, et al., for a teaching of the use of silicon carbide as an etch stop layer. However, this combination does not teach, suggest, or motivate the claimed capping layer on the surface of the conductor, and therefore this rejection is improper and should be reversed.

Rejection of Claim 16

Claim 16 has been rejected under 35 USC §103(a), as being unpatentable over Wolstenholme and Avanzino, et al., as applied to Claims 15, and further in view of Boeck, et al.

The combination of Wolstenholme, Avanzino, et al., and Boeck, et al., do not disclose, suggest, or provide motivation for the invention defined by Claim 16. More particularly, Applicants have shown that: Wolstenholme discloses a floating gate and not a conductor with a capping layer; Avanzino, et al., disclose an etch stop layer that is separated from the sidewalls of the conductor and not in contact therewith; and Boeck, et al., disclose a barrier layer and not a capping layer. The agglomeration of elements from this combination of references does not produce Applicants' claimed invention, nor do these references in any way suggest or motivate the invention set forth in Applicants' Claims. The improper rejection of Claim 16 should be reversed.

Conclusion

For the reasons set forth above, Applicants respectfully submit that the rejections of Claims 1 and 3-16 are improper and be reversed.

Respectfully submitted,

By Raymond J. Werner

Raymond J. Werner
Reg. No. 34,752

Dated: 29 September 2004
Hillsboro, Oregon

CLAIMS APPENDIX

1. (Previously Presented) A method of manufacturing an electronic device, a semiconductor device in particular but not exclusively, which method comprises the steps of:

applying a semiconductor substrate which is provided with a conductor at a surface, the conductor having a top surface portion and sidewall portions, of which at least the top surface portion is provided with an etch stop layer comprising silicon carbide;

applying a dielectric layer;

etching a via in the dielectric layer over the conductor, and stopping on the etch stop layer to create an exposed part of the etch stop layer;

removing the exposed part of the etch stop layer inside the via from at least the top surface portion of the conductor; and

filling the via with a conductive material;

wherein the etch stop layer is applied to the top surface portion and the sidewall portions of the conductor after the provision of the conductor at the surface of the semiconductor substrate.

2. (Cancelled)

3. (Previously Presented) A method as claimed in claim 1, characterized in that the via is etched while overhanging at least one of the sidewall portions of the conductor

and exposing at least part of the etch stop layer, which etch stop layer covers the top surface portion and the at least one of the sidewall portions of the conductor.

4. (Original) A method as claimed in claim 3, characterized in that the etch stop layer is removed from inside the via from only the top surface portion of the conductor.

5. (Previously Presented) A method as claimed in claim 1, characterized in that the etch stop layer is applied to the top surface portion and the sidewall portions of the conductor as well as to portions of the semiconductor substrate which are not covered by the conductor.

6. (Previously Presented) A method as claimed in claim 1, characterized in that the conductor is provided while comprised at least in part of a material selected from a group comprising aluminum, copper and tungsten.

7. (Previously Presented) A method as claimed in claim 1, characterized in that the conductor is provided comprising a capping layer, which capping layer provides the top surface portion of the conductor.

8. (Original) A method as claimed in claim 7, characterized in that the capping layer is comprised of a material selected from a group comprising titanium nitride, titanium tungsten and tantalum nitride.

9. (Previously Presented) A method as claimed in claim 1, characterized in that the dielectric is applied by depositing a dielectric material having a dielectric constant lower than that of silicon oxide.

10. (Original) A method as claimed in claim 9, characterized in that the dielectric layer is applied by depositing a material selected from a group comprising hydrogen silsesquioxane, parylene and a fluorinated polyimide

11. (Previously Presented) A method as claimed in claim 1, characterized in that the via is filled by depositing a conductive layer, which conductive layer comprises a metal selected from a group comprising aluminum, copper and tungsten.

12. (Previously Presented) The method of claim 1, wherein a capping layer immediately adjoins said etch stop layer.

13. (Previously Presented) A method of forming electrically conductive pathways, comprising:

forming a patterned conductor on a substrate, the patterned conductor having sidewalls and a top surface, the patterned conductor further having an electrically conductive capping layer disposed on the top surface thereof, the capping layer having a top surface and sidewalls;

forming a conformal etch stop layer such that the etch stop layer is in contact with at least the substrate, the sidewalls of the patterned conductor, and the top surface and sidewalls of the capping layer;

forming a dielectric layer over the etch stop layer;

forming a via opening in the dielectric layer, the via opening exposing a portion of the etch stop layer, the via opening at least partially overlapping the at least one patterned conductor;

anisotropically etching the exposed portion of the etch stop layer such that at least a portion of the capping layer is exposed; and

filling the via opening with electrically conductive material.

14. (Previously Presented) The method of Claim 13, wherein the via opening is unlanded, and wherein the electrically conductive material in the via opening is spaced away from the patterned conductor sidewalls and the capping layer sidewalls by the etch stop layer adjacent the sidewalls of the patterned conductor and the sidewalls of the capping layer.

15. (Previously Presented) The method of Claim 14, wherein the etch stop layer comprises silicon carbide.

16. (Previously Presented) The method of Claim 15, wherein the capping layer comprises a titanium layer disposed on the top surface of the patterned conductor,

and the capping layer further comprises a titanium nitride layer over the titanium layer.

EVIDENCE APPENDIX

NONE.

RELATED PROCEEDINGS APPENDIX

NONE.